DRONACHARYA
College of Engineering

KHENTAWAS, FARRUKHNAGAR, GURGAON, HR

Department: Electronics and Communication Engineering

Academic Session: 2017-18 (Jan-June 2018)

Lesson Plan for the Semester started w.e.f 08.01.2018

Subject with code: Digital System Design (EE-310-F)

Name of Faculty with designation : Ashish Gambhir (Assistant Professor)

Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Academic activity	Test / assignment
January		**VI-ECE/VI-CSE**	1	Importance of CAD Design Tools, Review of Digital Circuits and Systems	……	
January		**VI-ECE/VI-CSE**	1	Review of Digital Systems		**Assignment of 04 Ques. given**
January		**VI-ECE/VI-CSE**	1	Introduction to HDL and its difference from other Hardware Languages		
January		**VI-ECE/VI-CSE**	1	Data Objects & Classes in VHDL		**Assignment of 04 Ques. given**
January		**VI-ECE/VI-CSE**	1	Data Types in VHDL		
January		**VI-ECE/VI-CSE**	1	Operators and Operator Overloading in VHDL, Types of Delays		**Assignment of 07 Ques. given**
January		**VI-ECE/VI-CSE**	1	Demonstration of First Program in VHDL		
January		**VI-ECE/VI-CSE**	1	Entity and Architecture Declaration		
January		**VI-ECE/VI-CSE**	1	Introduction to behavioural, dataflow and structural models.		**Assignment of 05 Ques. given**
February		**VI-ECE/VI-CSE**	2	Assignment statements, sequential statements and process		
February		**VI-ECE/VI-CSE**	2	Conditional statements, case statement Array and loops		
February		**VI-ECE/VI-CSE**	2	Resolution functions, Packages and Libraries, concurrent statements		**Assignment of 08 Ques. given**
February		**VI-ECE/VI-CSE**	2	Application of Functions and Procedures		
February		**VI-ECE/VI-CSE**	2	Structural Modelling, component declaration		
February		**VI-ECE/VI-CSE**	2	Structural layout and generics		
February		**VI-ECE/VI-CSE**	3	VHDL Models and Simulation of combinational circuits of Mux and Demux		
March		**VI-ECE/VI-CSE**	3	VHDL Models and Simulation of combinational circuits of Encoders, Decoder		
March		**VI-ECE/VI-CSE**	3	VHDL Models and Simulation of combinational circuits of Code Converters		

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March		**VI-ECE/VI-CSE**	3	VHDL Models and Simulation of combinational circuits of Comparators		
March		**VI-ECE/VI-CSE**	3	Implementation of Sequential Circuits - Shift Registers, Counters		**Assignment of 08 Ques. given**
March		**VI-ECE/VI-CSE**	4	Basic components of a computer, specifications		
March		**VI-ECE/VI-CSE**	4	Architecture of a simple microcomputer system		
April		**VI-ECE/VI-CSE**	4	Implementation of a simple microcomputer system using VHDL		
April		**VI-ECE/VI-CSE**	4	Progr ammable logic devices : ROM, PLAs, PALs		**Assignment of 07 Ques. given**
April		**VI-ECE/VI-CSE**	4	GAL, PEEL		
April		**VI-ECE/VI-CSE**	4	CPLDs and FPGA		
April		**VI-ECE/VI-CSE**	4	Design implementation using CPLDs and FPGAs		**Assignment of 04 Ques. given**